

## **REMARKS**

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

### **I. Disposition of Claims**

Claims 1-10 were pending in the present application. By way of this reply, claims 1, 3, and 5 have been amended, claims 2 and 6-10 have been canceled without prejudice or disclaimer, and new claim 11 has been added. Accordingly, claims 1, 3-5, and 11 are currently pending in the present application.

### **II. Claim Amendments**

Claim 1 has been amended to recite that the plurality of signals generated by the counter stage sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current sourced from a power terminal to a ground terminal of the integrated circuit. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figures 2a and 2b of the present application.

Claim 3, which originally depended from now-canceled claim 2, has been amended to now depend from claim 1. No new matter has been added by way of this amendment.

Claim 5 has been amended to recite that the counter stage is arranged to generate a plurality of signals to a plurality of transistors connected in parallel across the power

terminal and the ground terminal. Further, claim 5 has been amended to recite that, dependent on the control signal, the plurality of signals are generated to sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current sourced from the power terminal to the ground terminal by the plurality of transistors. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figures 2a and 2b of the present application.

### **III. Rejection(s) Under 35 U.S.C § 102**

Claims 1-10 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,424,669 issued to Tegatz et al. (hereinafter "Tegatz"). By way of this reply, claims 2 and 6-10 of the present application have been canceled, and therefore, the rejection of these claims is now moot. With respect to remaining claims 1 and 3-5, for the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a technique for reducing the magnitude of current change when power consumption in an integrated circuit needs to be reduced. In prior art systems, when a power consumption reduction need arose in response to, for example, over-heating, current is instantly decreased (*i.e.*, the magnitude of current change is high). *See* Specification, paragraph [0003]. Such instant reduction in current leads to high magnitudes of voltage reduction, which may cause integrated circuit damage. *See* Specification, paragraph [0003].

With reference to the exemplary embodiment of the present invention shown in Figure 2a of the present application, a circuit in accordance with the present invention

causes a gradual reduction in current to occur in response to a power consumption reduction need. *See* Specification, paragraphs [0016], [0017]. When a power consumption reduction need arises, a control stage 30 generates a control signal **m\_out** to a counter stage 32, which, in turn, sequentially disables a plurality of transistors 34, 36, 38, 40 to cause a gradual reduction in the amount of current sourced from  $V_{DD}$  42 to  $V_{SS}$  44. *See* Specification, paragraphs [0016], [0017]. This gradual reduction in current is exemplarily shown in Figure 2b of the present application. In Figure 2b of the present application, the current sourced from  $V_{DD}$  42 to  $V_{SS}$  44 gradually decreases from 10 amperes to 5 amperes over time as the plurality of transistors 34, 36, 38, 40 are sequentially disabled by signals  $C_0$ ,  $C_1$ ,  $C_2$ ,  $C_3$  generated by the counter stage 32. *See* Specification, paragraphs [0015] – [0017].

Accordingly, independent claims 1 and 5 of the present application have been amended to require that the plurality of transistors be sequentially *disabled* to cause a *gradual reduction* in an amount of current sourced from a power terminal to a ground terminal.

Teggatz, in contrast to the present invention, fails to disclose all the limitations recited in amended independent claims 1 and 5 of the present application. In Teggatz, in order to incrementally adjust an output impedance of a power device (*see* Teggatz, column 1, lines 42 – 64), a plurality of transistors in the power device are *enabled* to cause an *increase* in an amount of sourced current. For example, as shown in Figures 2 and 3 of Teggatz, transistors 25, 27, 29, 31, 33 in the power device 24 are sequentially turned “on” or enabled to cause a gradual increase in current flow between power and ground. *See* Teggatz, column 3, lines 15 – 60. This gradual increase in current is evident

in Figure 3 of Tegatz, which shows current  $I_{DS}$  gradually increasing as the transistors 25, 27, 29, 31, 33 are sequentially turned “on” or enabled.

Thus, Tegatz discloses sequentially *enabling* current sources (*e.g.*, transistors connected between power and ground) to cause a gradual *increase* in an amount of current sourced from power to ground, whereas the claimed invention requires sequentially *disabling* current sources to cause a gradual *reduction* in an amount of current sourced from power to ground. Accordingly, Tegatz fails to disclose all the limitations of amended independent claims 1 and 5 of the present application.

In view of the above, Tegatz fails to show or suggest the present invention as recited in amended independent claims 1 and 5 of the present application. Thus, amended independent claims 1 and 5 of the present application are patentable over Tegatz. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

#### IV. New Claim


By way of this reply, new claim 11 has been added. New claim 11 recites that when the plurality of transistors are enabled, the plurality of transistors source substantially a maximum amount of current from the power terminal to the ground terminal. No new matter has been added by way of new claim 11 as support for new claim 11 may be found, for example, in Figures 2a and 2b of the present application. Accordingly, entry and favorable treatment of new claim 11 is respectfully requested.

#### V. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.106001;P6086).

Respectfully submitted,

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